Mike Banning

Dan Keating

CSE 557 – Assignment 2 – HyperQuicksort

3/13/2012

1. **Discovering the cache sizes and latencies at multiple memory hierarchy levels**
   1. Cache size and average access latencies

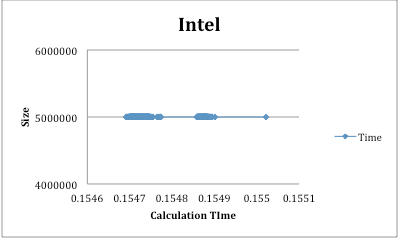
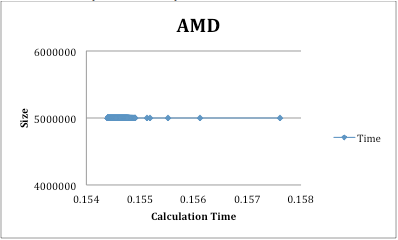
Size growth was limited to 5,000,000 for calculations due to time of execution. The graphs presented here were limited to 500,000 because growth becomes linear, and the earlier cache latencies don’t show up.

Cache sizes

|  |  |  |  |
| --- | --- | --- | --- |
|  | L1 | L2 | Main Memory |
| AMD |  |  |  |
| Intel |  |  |  |

Average per word access latencies

|  |  |  |  |
| --- | --- | --- | --- |
|  | L1 | L2 | Main Memory |
| AMD |  |  |  |
| Intel |  |  |  |

* 1. Random memory access latency  
       
     Is the average random access latency the same as the numbers for memory access in part 1?

2) **Discovering communication latencies**calculate the average and median round trip latencies for a single message?  
what is the one-way latency? discuss

3) **Discovering communication bandwidth and startup costs**Does the scatter plot follow the [ts and tw slope] line?

Calculate the bandwitdths for both plots?

**4) Fitting a model to execution times of parallel quicksort**can you fit a function to model T(N,P)?

What is the function?

Are the errors acceptable? If not, will more than one model help?

Explain in one paragraph how a model like this could be used for performance optimizations?