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CSE 557 – Assignment 2 – HyperQuicksort

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1. **Discovering the cache sizes and latencies at multiple memory hierarchy levels**
   1. cache size and average access latencies  
      estimate cache sizes for Intel and AMD?  
      use number of operations to determine the average per word access latencies to each ache level and main memory?
   2. random memory access latency  
      Is the average random access latency the same as the numbers for memory access in part 1?

2) **Discovering communication latencies**calculate the average and median round trip latencies for a single message?  
what is the one-way latency? discuss

3) **Discovering communication bandwidth and startup costs**Does the scatter plot follow the [ts and tw slope] line?

Calculate the bandwitdths for both plots?

**4) Fitting a model to execution times of parallel quicksort**can you fit a function to model T(N,P)?

What is the function?

Are the errors acceptable? If not, will more than one model help?

Explain in one paragraph how a model like this could be used for performance optimizations?